

RTX64

Tested Processor Compatibility

This document outlines compatibility between supported RTX64 versions and the system processors that were available for testing as part of the IntervalZero QA test lab. Note that other processors should work. To request that a specific processor be added to our QA test lab, please contact support@intervalzero.com.

NOTE: The Windows operating system installed on the machine must support the hardware.

KEY



The processor was available to the QA team and was tested with the RTX64 version. No issues were found during testing.



The processor was not available to the QA team and was not tested with the RTX64 version. The processor should work with RTX64, but IntervalZero does not claim compatibility.



The processor was tested and determined to be not compatible with the RTX64 version.

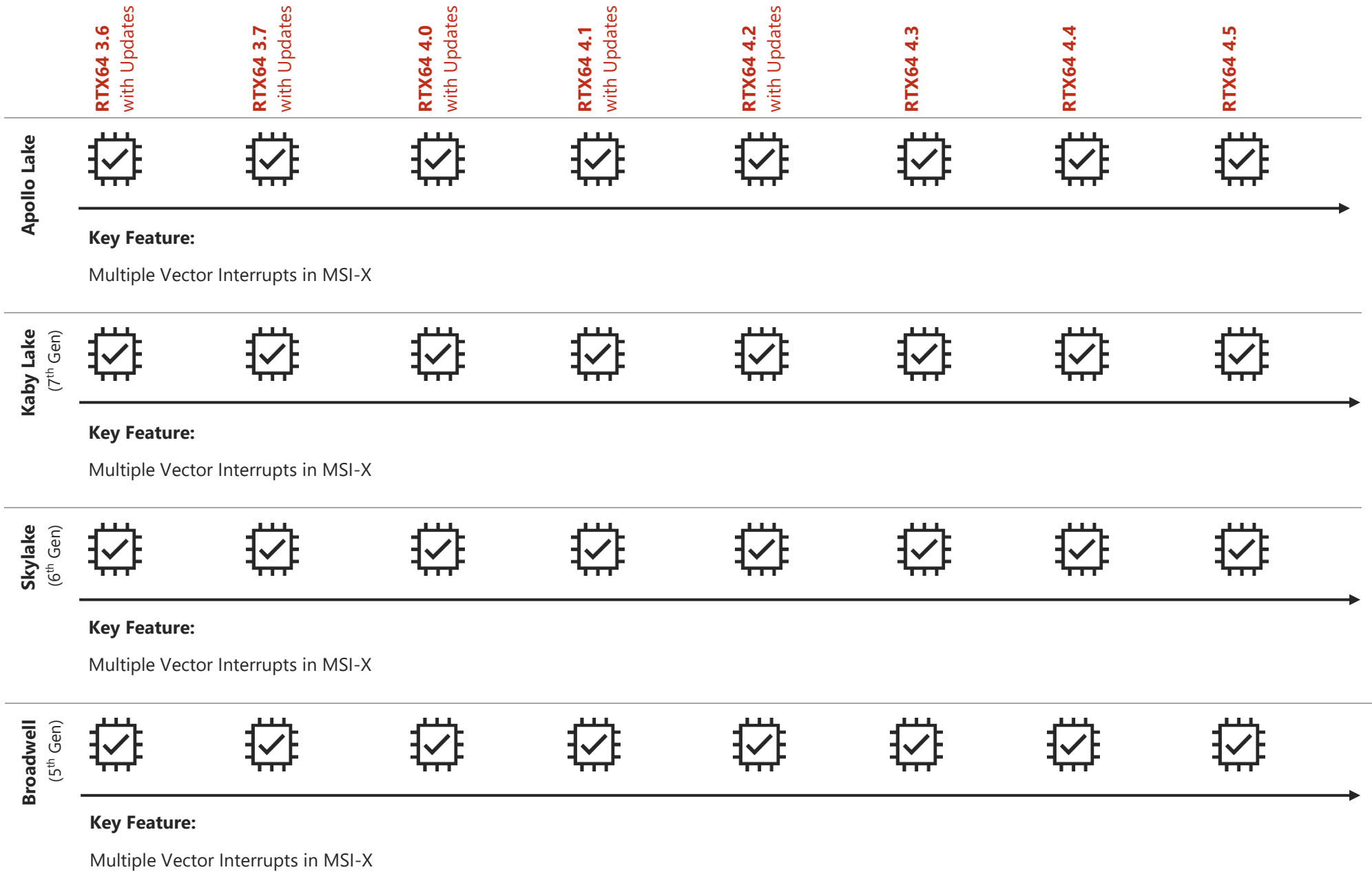
RTX64 3.6-4.5

	RTX64 3.6 with Updates	RTX64 3.7 with Updates	RTX64 4.0 with Updates	RTX64 4.1 with Updates	RTX64 4.2 with Updates	RTX64 4.3	RTX64 4.4	RTX64 4.5
Elkhart Lake (Atom 6 th Gen x6000E)					 RTX64 4.2.1			
Key Features: Intel® Hybrid CPU Cores (E-cores and P-cores); Intel® Thread Director; Intel® Control-flow Enforcement Technology								
Raptor Lake (13 th Gen)					 RTX64 4.2.1			
Key Features: Intel® Hybrid CPU Cores (E-cores and P-cores); Intel® Thread Director; Intel® Control-flow Enforcement Technology								
Alder Lake (12 th Gen)					 RTX64 4.2.1			
Key Features: Intel® Hybrid CPU Cores (E-cores and P-cores); Intel® Thread Director; Intel® Control-flow Enforcement Technology								









	RTX64 3.6 with Updates	RTX64 3.7 with Updates	RTX64 4.0 with Updates	RTX64 4.1 with Updates	RTX64 4.2 with Updates	RTX64 4.3	RTX64 4.4	RTX64 4.5
Haswell (4 th Gen)								

Key Feature:

Multiple Vector Interrupts in MSI-X

Ivy Bridge (3 rd Gen)								
--	--	--	--	--	--	--	--	--

Windows 10:

RTX64 3.6.2
requires the
latest Windows
10 KB updates.

Key Feature:

Multiple Vector Interrupts in MSI-X

Sandy Bridge (2 nd Gen)								
--	--	--	--	--	--	--	--	--

Key Feature:

Multiple Vector Interrupts in MSI-X